AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions of claims in the application.

Claim 1 (Currently Amended): An A/D conversion array comprising arrayed unit circuits, each of which ~~comprising~~ comprises:

~~a circuit element for performing N-bits of A/D conversion per cycle;~~

~~a circuit element for D/A converting the digital output of said circuit element by first switching means and a first capacitor;~~

~~amplification means for connecting a second capacitor for determining gain by a ratio with said first capacitor between the input and output of an inverting amplifier for subtracting the analog value of said conversion result from the analog input and for amplification of the analog input;~~

~~a circuit element for sampling and holding the output of said amplification means by second switching means and said first capacitor; and~~

~~third switching means for selecting one of output of said amplification means and an input signal and supplying the selected signal to said amplification means as input, via said first capacitor, the A/D conversion array being characterized in that~~

~~control means for said first to third switching means is installed outside the array, an input signal is supplied as the input of said amplification means in the first stage, and a signal through said sample and hold circuit element is supplied to the input of said amplification circuit in the next stage, whereby cyclic multi-bit A/D conversion is performed~~

a first circuit element arranged to perform A/D conversion of multiple bits per cycle;

a second circuit element arranged to convert a digital output of said first circuit element to a resulting analog conversion signal by first switching means, and

a first capacitor;

amplification means arranged to amplify an analog input, the amplification means comprising a second capacitor for determining gain from a ratio of capacitance of the second capacitor and said first capacitor, the second capacitor being connectable between an input and an output of an inverting amplifier to subtract the analog conversion signal from the analog input;

a third circuit element arranged to sample and hold an output of said amplification means by second switching means and said first capacitor; and

third switching means arranged to select one of the output of said amplification means and an input signal and to supply the selected signal to said amplification means as input, via said first capacitor, the A/D conversion array being characterized in that:

control means arranged to control said first to third switching means is installed outside the array, and the arrayed unit circuits are arranged such that cyclic multi-bit A/D conversion is performed when the input signal is supplied as an input of said amplification means in a first stage, and a signal from said third circuit element is supplied to the input of said amplification means in a next stage.

Claim 2 (Currently Amended): The A/D conversion array according to Claim 1, ~~characterized in that~~ wherein two first capacitors ~~used for D/A conversion by said amplification means, are installed connected to an input terminal of said amplifier, and the conversion speed~~

~~per cycle is doubled by alternately using said plurality of first two capacitors for D/A conversion and for sampling and holding~~ are arranged to be used for D/A conversion with said amplification means, and a conversion speed per cycle is doubled by alternately using said two first capacitors for D/A conversion and for sampling and holding.

Claim 3 (Currently Amended): The A/D conversion array according to Claim 1, ~~characterized in that~~ wherein said circuit element ~~for performing N-bits of A/D conversion divides the analog signals, which are input, into three areas depending on a voltage level, and assigns the values 1, 0 and -1 to the three areas~~ arranged to perform A/D conversion of N-bits is arranged to divide input analog signals into three voltage ranges, and to assign values 1, 0 and -1 to the three ranges.

Claim 4 (Currently Amended): The A/D conversion array according to Claim 1, ~~characterized in that~~ wherein an amplifier in said amplification means is a differential amplifier having a differential input and a differential output, and a full differential circuit is structured by said differential amplifier, a capacitor and switching means ~~in the peripheral area thereof~~.

Claim 5 (Currently Amended): An image sensor, ~~characterized by performing A/D conversion in parallel for the output of an image sensor array by arranging the A/D conversion array according to any one o Claim 1 to Claim 4 in a column of the image sensor array~~ arranged to perform A/D conversion in parallel for outputs of elements of an image sensor array thereof

comprising an A/D conversion array as claimed in any one of Claims 1 to 4 located in a column of the image sensor array.

Claim 6 (Currently Amended): The image sensor according to Claim 5, further comprising a noise cancellation circuit in a column of said image sensor array, ~~characterized in that~~ wherein said noise cancellation circuit comprises ~~a second inverting amplifier, a third capacitor connected between the output of the image sensor array and the input of said second inverting amplifier, and a fourth capacitor connected between the input and output of said second inverting amplifier, and switching means for switching connections of these elements, and the inverting amplifier in said cyclic A/D conversion array is also used as the second inverting amplifier of said noise cancellation circuit, said first capacitor is also used as said third capacitor, and said second capacitor is also used as said fourth capacitor~~ a noise cancellation inverting amplifier, a first noise cancellation capacitor connected between the output of the image sensor array and the input of said noise cancellation inverting amplifier, and a second noise cancellation capacitor connected between the input and output of said noise cancellation inverting amplifier, and switching means arranged such that, and the inverting amplifier in said A/D conversion array is also arranged to be used as the noise cancellation inverting amplifier of said noise cancellation circuit, said first capacitor is also arranged to be used as said first noise cancellation capacitor, and said second capacitor is also arranged to used as said second noise cancellation capacitor.

Claim 7 (Currently Amended): The image sensor according to Claim 6, further comprising a fifth capacitor ~~as a capacitor to be connected between the output of the image~~

~~sensor array and input of the inverting amplifier only during a noise cancellation operation, characterized in that an amplification function is acquired by the capacity ratio with said second capacitor~~ arranged to be connected between the output of the image sensor array and input of the inverting amplifier only during a noise cancellation operation, characterized in that an amplification function is acquired by a ratio of a sum of the capacitance of the first capacitor and the third capacitor with said second capacitor.